

PATENTAmendments to the Specification:

Please replace the paragraph beginning on Page 3, Line 13 with the following amended paragraph:

Figure 1 shows a high-level block diagram of the present central/peripheral processor system architecture 100 for packet processing. Central processor 110 receives packets through any of a number of means well-known in the art. ~~central~~ Central processor 110 performs, in some embodiments, preliminary format checking, e.g., checksum validation, and passes the packet or parts of the packet to one or more peripheral processors for additional work. ~~central~~ Central processor 110 may pass data to one or more peripheral processors 120, 130, 140, and 150 in sequence, in parallel, or in a pipelined fashion.